14.5 A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS

Xun Sun, Akshat Boora, Wenbing Zhang, Venkata Rajesh Pamula, Visvesh Sathe

University of Washington, Seattle, WA

Low-Dropout Regulators (LDOs) play an important role in enabling fine-grained supply-voltage domains for energy-efficient SoC design [1]. Digital LDOs are of particular interest due to integration and scalability advantages, but their transient response is slowed down by intrinsic limitations in sampled feedback systems. Design margins to ensure stability across worst-case PVT conditions further degrade transient response. Meanwhile, voltage domains continue to shrink in size, thus mandating a faster LDO response to compensate for reduced available decoupling capacitance (decap).

Recently reported non-linear control and event-driven architectures offer fast recovery times [2] [3]. However, non-linear approaches face the challenge of ensuring stable mode transitions under random load current (I_L) conditions. Event-driven LDOs trigger logic to control MOS devices based on threshold crossings made by the regulated voltage (V_{out}). However, typical digital systems exhibit constant load fluctuation, which can result in prohibitive switching losses. To address the impact of worst-case margining, adaptive LDO designs have also been proposed, but they largely focus on suppressing V_{out} ripple [4], and compensating for load current variation [5].

This paper presents computational regulation, a technique for fast and stable transient response across PVT. This concept is demonstrated in a Digital LDO that drives a Cortex-M0 processor with an integrated linear algebra accelerator (Fig. 14.5.1). The key idea is to: 1) derive time-domain models that are more accurate than those obtained from the traditional discrete-time transfer function and 2) evaluate the resulting state equations at runtime for rapid regulator response. We also introduce Autonomous Gain Tracking (AGT), a low-overhead, low-complexity technique that examines V_{out} statistics for runtime loop-gain tuning to enable rapid LDO response across PVT. In any cycle *n*, the LDO samples and quantizes the error voltage $\Delta V[n] = V_{out}[n] - V_{ref}$. A *Solver* then uses $\Delta V[n]$ to evaluate LDO state equations to determine *k[n]*, the number of PMOS devices to be turned-on in the same cycle. Ideally, *k[n]* is selected to meet I_L requirements and restore V_{out} within one LDO cycle. To determine *k[n]*, the *Solver* requires a well-tuned gain term, $G_S = C_L/(I_0 T)$ (Fig. 14.5.1) that captures important design parameters. These parameters include: 1) I_0, the current delivered by a unit LDO PMOS device, 2) C_L, the V_{out} decap, and 3) T, the LDO clock period. G_S is therefore sensitive to PVT variation and must be tracked for rapid, robust response. AGT monitors the LDO loop gain and subsequently adjusts G_S to maintain speed and stability.

Figure 14.5.2 details the LDO architecture. The error between V_{out} and V_{ref} is first quantized by 13 clocked comparators. Non-uniform quantization offers a more effective trade-off between resolution and range [6]. To achieve sub-cycle loop delay, the LDO updates the number of conducting PMOS devices immediately after the *Solver* determines *k[n]*. Both comparator and *Solver* outputs are latched using suitably delayed clocks to provide sufficient evaluation time for each module. Although this approach suppresses loop delay to a fraction of the LDO clock (αT_{LDO}), loop delay is not eliminated. Consequently, the effective number of conducting PMOS devices in cycle *n* depends on both *k[n]* and *k[n-1]*, an effect that needs to be modeled in fast LDOs. The implemented LDO *Solver* (Fig. 14.5.2) incorporates this dependence for improved droop response and stability.

Rapid, stable LDO operation requires good matching of G_S between that modeled by the solver ($G_{S,model}$) and the actual PVT-dependent G_S ($G_{S,actual}$). Any mismatch degrades either LDO stability or speed. The AGT loop (Fig. 14.5.3) acts as a low-bandwidth digital servo that uses the lag-1 autocorrelation of V_{out}, R[1], to characterize the LDO response and suitably update $G_{S,model}$ to track $G_{S,actual}$. Fig. 14.5.3 shows how the sign of R[1] reflects LDO response: a negative (positive) value of *R[1]* suggests an under-damped (over-damped) I_L step response, indicating that $G_{S,model} > G_{S,actual}$ ($G_{S,model} < G_{S,actual}$). *R[1]* = 0 indicates an ideal response with no G_S mismatch. This relationship can be proven to extend beyond a unit-step load to random runtime current loads. Because only the sign of R[1] is needed, the AGT performs a bit-wise XOR of the MSBs of successive $\Delta V[n]$ values. An up-down counter accumulates the XOR result over 40 samples to account for statistical variation. Accumulated totals with sufficient magnitude reflect a systematic positive or negative trend in *R[1]*, causing the loop to update G_S.

The proposed LDO was fabricated in a low-power 65-nm CMOS process. All modules, except the PMOS header devices and comparators, were synthesized. The load current is provided by processor/accelerator execution and an on-chip I_L step generator. The test-chip die photograph is shown in Fig. 14.5.7. 250pF of decap was added to V_{out}. Both processor and accelerator operate at the same frequency.

Figure 14.5.4 shows the measured LDO response to a 5.6mA/100ps I_L load step. Also shown is the response obtained by separately disabling loop-delay modeling and AGT. The responses were obtained under nominal conditions (V_{in}=1.1V, V_{out}=1.0V) after allowing the AGT loop to track G_S during processor execution—no manual tuning of *Solver* parameters was performed. The LDO requires very few cycles to settle, achieving a mean settling time of 2.79 cycles. Single-cycle settling requires addressing variation in the alignment between the load step and LDO clock edges, as well as non-uniform quantization. Without loop-delay modeling, both droop response and stability are degraded. With V_{in}=1.1V, V_{out} was then scaled by 150mV to 0.85V under two scenarios: with and without enabling AGT. AGT allows a near-ideal step response at V_{out} = 0.85V. Without AGT, however, the LDO is unstable. The 150mV V_{out} reduction requires reducing G_S by 50% to stabilize the loop which in turn doubles the measured voltage droop at V_{out} = 1.0V.

Figure 14.5.5 shows the AGT loop modifying $G_{S,model}$ to track $G_{S,actual}$ by examining V_{out} statistics during processor execution. The experiment was repeated using three distinct initial $G_{S,model}$ values. Each point on the curve represents a G_S update based on a 40-sample R[1] accumulation. All three curves converge to a common level that lies within 10% of the optimal G_s. Measurements indicate that the AGT successfully performs the broad gain adjustments needed for consistently fast transient response across variation in V_{in}, V_{out} and temperature. These broad adjustments demonstrate the impact of margins on transient response.

Measured load regulation for V_{in} in the 0.65-to-1.0V range and regulator current efficiency are shown in Fig. 14.5.6. Also included is a comparison to related prior work. Regulator switching losses are dominated by *Solver* dynamic power and effectively amortized in designs with higher I_L. AGT losses make up only 5% of total LDO switching losses.

Computational Regulation presents a new approach to exploiting advances in computing performance and efficiency to realize LDOs with stable and fast transient response across PVT. The proposed autocorrelation-based autonomous gain tracking architecture tracks PVT-induced gain variations, reducing required stability margins and consistently enabling rapid transient response. Computational regulation is expected to offer enhanced efficiency and performance in advanced CMOS nodes.

Acknowledgments:
The authors thank Nasser Kurd, Praveen Mosalikanti, Carlos Tokunaga, Alvin Loke and Sanjay Pant for their valuable input. Funding for this work was provided by grants from Intel, and from SRC (TxACE) under grant No. 2712.006.

References:

[1] Z. Toprak-Deniz, et al., "Distributed System of digitally Controlled Microregulators Enabling Per-Core DVFS for the POWER8TM Microprocessor," *ISSCC,* pp. 98-99, 2014.
[2] T. Mahajan, et al., "Digitally Controlled Voltage Regulator Using Oscillator-Based ADC with Fast-Transient-Response and Wide Dropout Range in 14nm CMOS," *CICC*, pp. 1-4, 2017.
[3] D. Kim, et al., "A 0.5V-VIN1.44mA-class Event-Driven Digital LDO with a Fully Integrated 100pF Output Capacitor," *ISSCC*, pp. 346-347, 2017.
[4] W. Tsou, et al., "Digital Low-Dropout Regulator with Anti PVT-Variation Technique for Dynamic Voltage Scaling and Adaptive Voltage Scaling Multicore Processor," *ISSCC,* pp. 338-339, 2017.
[5] S. B. Nasir, et al., "A 0.13µm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range," *ISSCC*, pp. 1-3, 2015.
[6] H. Hu, et al., "Nonuniform A/D Quantization for Improved Dynamic Responses of Digitally Controlled DC–DC Converters," *IEEE Transactions on Power Electronics,* vol. 23, no. 4, pp. 1998-2005, 2008.

 978-1-5386-8531-0/19/$31.00

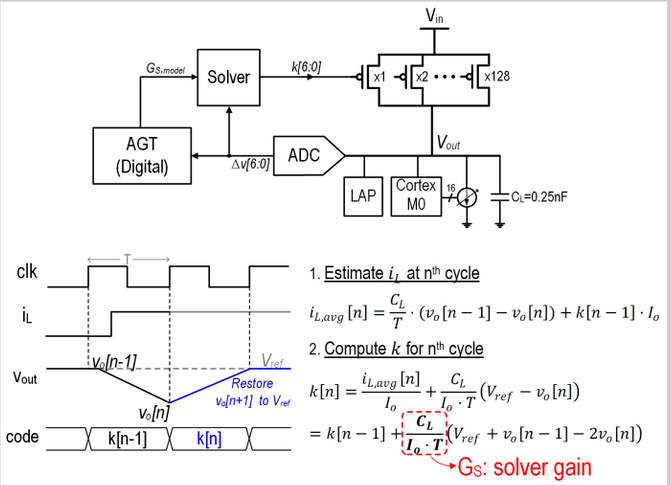


Figure 14.5.1: A computationally regulated digital LDO with low-bandwidth Autonomous Gain Tracking (AGT) loop. Intended operation and simplified equations.

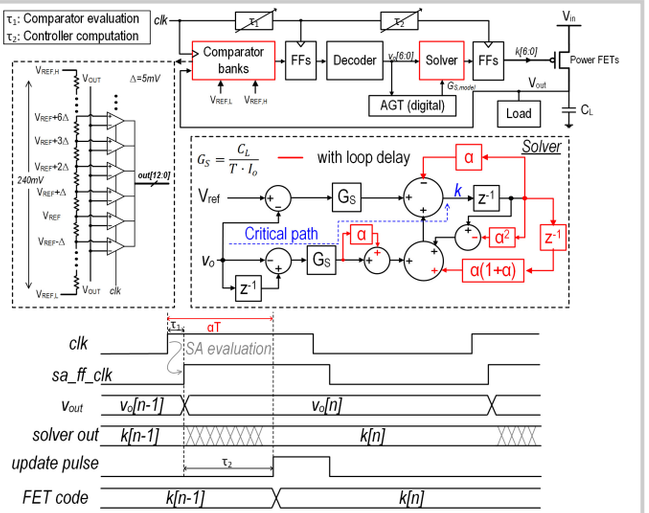


Figure 14.5.2: Detailed LDO block diagram and timing diagram of same-cycle update using sub-cycle (αT) loop delay.

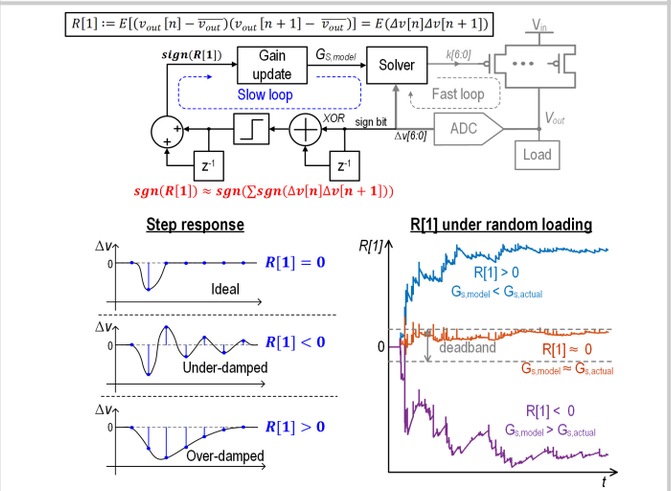


Figure 14.5.3: AGT tracks loop gain across PVT. The lag-1 auto-correlation (R[1]) sign effectively characterizes loop gain for $G_{S,model}$ update under load I_L step and random load conditions.

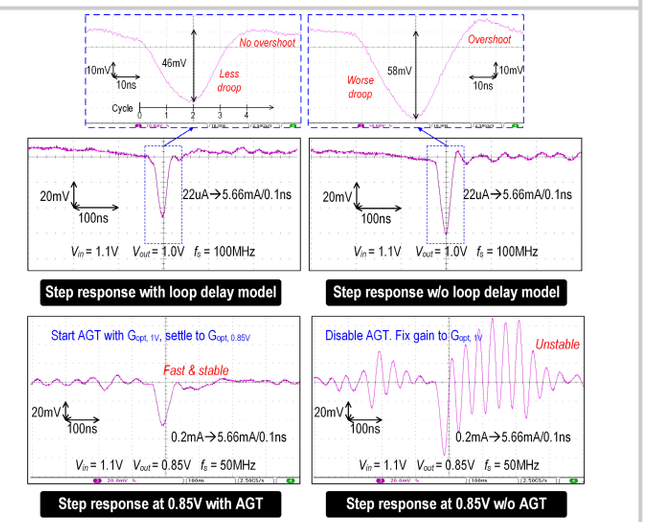


Figure 14.5.4: Measured LDO step-response under regular operating configuration, and with loop-delay modeling and AGT separately disabled.

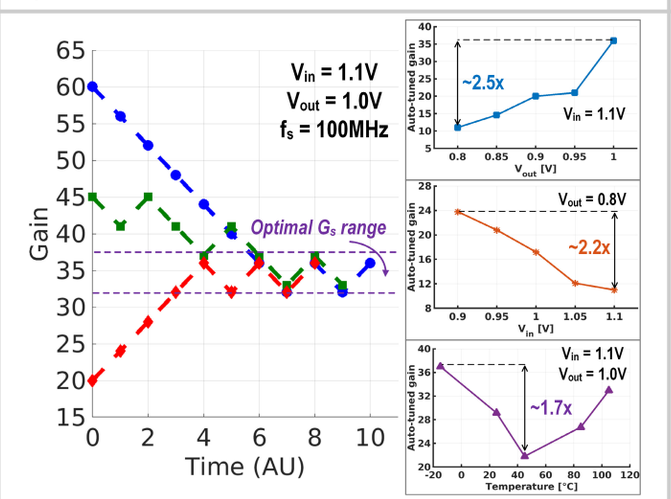
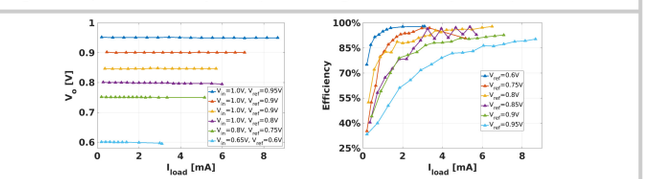


Figure 14.5.5: (Left) Runtime $G_{S,model}$ traces converging to $G_{S,actual}$ from distinct incorrect initial values. (Right) Measured $G_{S,model}$ across different V_{out}, V_{in} and temperature indicate the need for significant adjustment.



Paper	[2]	[3]	[4]	[5]	This work
Process	14nm	65nm	40nm	130nm	65nm
Type	Digital	Digital	Digital	Digital	Digital
Control topology	Time-driven	Event-driven	Time-driven	Time-driven	Time-driven
Control type	Linear (type-2) + non-linear	Linear PI	Linear PID	Linear PI + RDS	Computational (digital)
Autonomous PVT tracking	No	No	Yes[1]	No	Yes
V_{in} [V]	1 – 1.15	0.45 – 1	0.6 – 1.1	0.5 – 1.2	0.65 – 1.15
V_{out} [V]	0.5 – 1.12	0.4 – 0.95	0.5 – 1	0.45 – 1.14	0.6 – 1.1
Max I_{LOAD} [mA]	2200	1.44	210	4.6	16.3
C_L [nF]	18	0.1	20	1	0.25
I_Q [µA]	14960[2]	8.1 – 258	22.6 – 98.5	24 – 221	80 – 1200[3]
F_{sample} [MHz]	400 (linear) 800 (nonlinear)	N/A	N.R.	5 - 75	16 – 100
ΔV_{out} [mV] @ ΔI_{LOAD} / T_{EDGE}	100mV @ 1A/10ns	34mV @ 1.44mA	36mV @ 200mA	40mV @ 0.7mA	46mV @ 5.6mA/0.1ns
Droop settling cycle (absolute time)	11.36[4] (14.6ns)	N/A (11200ns)	N.R. (13000ns)	33[4] (1100ns)	2.79[5] (27.9ns)

[1] Tracking for output voltage ripples only [2] Calculated from efficiency data
[3] Measured under realistic conditions and dominated by controller switching power, which does not appreciably increase with I_{LOAD} increase
[4] F_{sample} during transient response used for calculation [5] Mean value across 100 random iterations

Figure 14.5.6: (Top) Load regulation and Current efficiency. (Bottom) Comparison with related works.

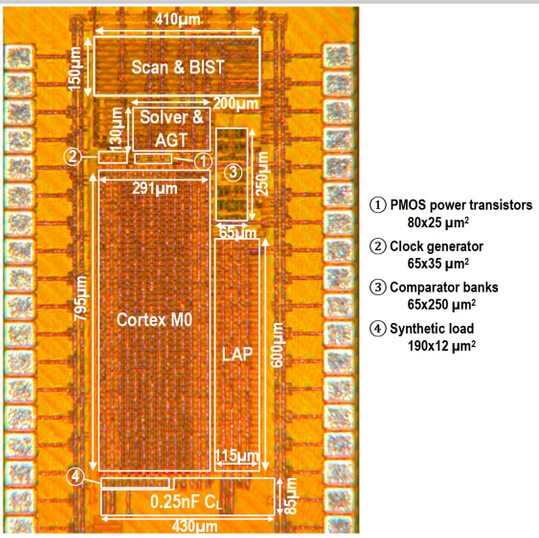


Figure 14.5.7: Die photograph of the LDO, implemented in 65nm CMOS.

978-1-5386-8531-0/19/$31.00 ©2019 IEEE